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An efficient comparative concurrent Built-In Self-Test technique

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Abstract: Built-In Self-Test (BIST) techniques constitute an attractive and practical solution to the difficult problem of testing VLSI circuits and systems. Among the BIST techniques the Comparative Concurrent BIST (C-BIST) has various advantages since it provides for off-line test generation, when it is desirable, and thus accomplishes a mixed on-line/off-line BIST scheme. However, in C-BIST when the test sequence is long, the time required for all the test vectors to appear among the normal inputs to the circuit (test latency) is significantly long. Modifications of the C-BIST technique have been proposed in order to reduce the test latency. In this paper we propose a new C-BIST technique termed windowed-CBIST (w-CBIST) for test latency reduction. The proposed technique is shown to be significantly more efficient from the previous methods with respect to test latency and hardware overhead.