2006

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IEEE Xplore

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Abstract

Today's nanometer technology trends have a very negative impact on the reliability of semiconductor products. Intermittent faults constitute the largest part of reliability failures that are manifested in the field during the semiconductor product operation. Since Software-Based Self-Test (SBST) has been proposed as an effective strategy for on-line testing of processors integrated in non-safety critical low-cost embedded system applications, optimal test period specification is becoming increasingly challenging.

In this paper we first introduce a reliability analysis for optimal periodic testing of intermittent faults that minimizes the test cost incurred based on a two-state Markov model for the probabilistic modeling of intermittent faults. Then, we present for the first time an enhanced SBST strategy for on-line testing of complex pipelined embedded processors. Finally, we demonstrate the effectiveness of the proposed optimal periodic SBST strategy by applying it to a fully-pipelined RISC embedded processor and providing experimental results.

1. Introduction

Current semiconductor fabrication processes for nanometer technology have a very negative impact to manufacturing yield and in-field reliability. The reliability faults manifested in the field during the life cycle of semiconductor products are classified in the following three types. *Permanent faults* reflect irreversible physical changes. Improvements in semiconductor design and manufacturing have significantly decreased the occurrence of permanent faults. *Intermittent faults* appear repeatedly at the same location causing errors in bursts when they are active, because of unstable or marginal hardware mainly due to process variations and manufacturing residuals. *Transient faults* (also known as "soft-errors") appear irregularly at various locations and last short time. These faults are induced by temporary environmental conditions such as neutron and alpha particles, power supply and interconnect noise, electromagnetic interference and electrostatic discharge.

Concurrent error detection, self-checking, time and space redundancy mechanisms that significantly increase system cost [1] are not suitable for non safety-critical low-cost embedded system applications. In such embedded applications detection of intermittent operational faults, that cause errors in bursts only when they are active and may precede the occurrence of permanent faults, is much more important than detection of transient operational faults that appear once and last short time.

On-line periodic testing is a non-concurrent test strategy, well suited to such embedded systems since it provides low-cost detection of permanent and intermittent faults with very high probability, that trades off between fault detection latency and performance overhead.

On-line periodic testing of deeply embedded processors in complex low-cost and non safety-critical embedded systems is becoming increasingly challenging. Hardware-based built-in self-test (BIST) techniques for on-line periodic testing provide excellent test quality and at-speed testing at the cost of increased hardware overhead, high power consumption and manual extensive design changes. Software-based self-test (SBST) in several variations on [2]-[9] has been proposed as a very promising approach for at-speed processor testing using low-cost structural testers. SBST is a non-intrusive approach that utilizes processor resources and Instruction Set Architecture (ISA) to perform test generation, test application and test response evaluation. Recently, the use of low-cost SBST techniques for on-line periodic testing of embedded processors has been proposed in [8] as an effective alternative solution to hardware-based BIST.

In this paper first we present a reliability analysis of intermittent faults (also including permanent faults) using probabilistic modeling. For on-line periodic testing of embedded processors, we introduce a novel cost function in order to minimize the test cost incurred by the execution of SBST programs and achieve high detection probability. Then, we present for the first time an enhanced SBST strategy for on-line periodic testing of embedded pipelined processors with more advanced ISA than the publicly available benchmarks used so far (e.g. [2],[3],[4],[7],[8]) and demonstrate the effectiveness by applying it to a fully-pipelined RISC embedded processor.

3-9810801-0-6/DATE06 © 2006 EDAA