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Accumulator-based built-in self-test generator for robustly detectable sequential fault testing

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Abstract: In this paper an algorithm for the generation of single input change (SIC) pairs is presented, termed the accumulator-based SIC pair generation (ASG) algorithm; SIC pairs have been effectively utilised for testing robustly detectable sequential faults. ASG is implemented in hardware utilising an accumulator whose inputs are driven by a barrel shifter. Since such structures (accumulators whose inputs are driven by barrel shifters) are commonly found in current, high-speed signal processing VLSI circuits, the presented schema provides a practical solution for the built-in testing of such circuits for testing delay and stuck-open faults. Utilisation of ASG to applying SIC pairs to adjacent pairs of inputs of the CUT, resulting in pseudoexhaustive schemes, is also addressed.

1 Introduction

In current IC technology, where highly complex chips have low accessibility of internal nodes, traditional testing becomes costly and ineffective; built-in self test (BIST) techniques have been proposed as an efficient alternative to external testing. BIST employs on-chip test generation and response verification; thereby the need for expensive external testing equipment is greatly reduced. Furthermore, with BIST at-speed testing can be achieved and the quality of the delivered ICs is highly increased [1].

Exhaustive testing provides 100% fault coverage of detectable single and multiple stuck-at faults without the need for fault simulation or deterministic test pattern generation. However, a large class of physical defects do not map into these fault categories. A transistor stuck-open fault in a CMOS circuit can convert a combinational Circuit Under Test (CUT) into a sequential one [2]. On the other hand, a delay fault does not affect the steady-state operation, but may cause circuit malfunction at clock speed [3, 4]. Detection of such faults requires two-pattern tests.

In the literature, several two-pattern BIST generators have been presented, e.g. [5–14]. Dufaza and Zorian [5] devised algorithms to generate deterministic two-pattern tests utilising LFSRs. Craig [6], Wang [7], and Girard [8] presented BIST techniques to detect an important class of path delay faults, called robustly detectable faults [6]. In [9, 10] two-pattern test generation using cellular automata was investigated.

Two largely known types of patterns have been investigated in the literature, Multiple Input Change (MIC) pairs and Single Input Change (SIC) pairs.

SIC pairs are pairs of patterns in which the first pattern of the pair differs from the second in exactly one bit. In the literature, it has been shown that SIC pairs hold some very interesting properties, thus a number of techniques have been presented for the generation of SIC pairs in a BIST environment e.g. [6–8, 11, 15–22]. In Section 2, the particular usefulness of SIC pairs for the detection of delay faults is discussed and justified.

Accumulators commonly exist in current VLSI circuits, e.g. in data path architectures, or in Digital Signal Processing chips, [23, 24]. Utilising accumulators for Built-In Testing (compression of the CUT responses [25–28], or generation of test patterns [29–32]) results in low hardware overhead and low impact on the circuit normal operating speed. However, the techniques that have been presented in the literature target either the detection of stuck-at faults [29–31], or the generation of MIC two-pattern tests [32], hence they are not suitable for the generation of SIC pairs.

Pseudo-exhaustive testing has been widely accepted as a means of decreasing the number of test patterns required for the testing of combinational CUTs [29]. The problem of generating pseudo-exhaustive test patterns has been widely investigated, e.g. [33–35]. However, pseudo-exhaustive testing for two pattern tests has been addressed only for the generation of Multiple Input Change pairs [36].

In this paper a technique is presented for the generation of SIC pairs of patterns, termed Accumulator-based SIC pair Generation (ASG). ASG is implemented in hardware utilising an accumulator whose inputs are driven by a barrel shifter. Such structures are commonly found in typical DSP cores (Fig. 1). Pseudo-exhaustive generation of SIC pairs is also addressed.

2 SIC pairs for two-pattern testing

SIC pairs are pairs of patterns in which the first pattern differs from the second in exactly one bit. The utilization of SIC pairs for the detection of stuck-open and delay faults holds some very interesting properties and has been approached by a number of researchers both theoretically [37] and experimentally [4, 15–22]. In the theoretical field,