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A Concurrent Built-In Self-Test Architecture Based on a Self-Testing RAM

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Index Terms—Built-in self-testing, concurrent testing, input vector monitoring.

SUMMARY AND CONCLUSIONS

Manufacturing test is carried out once to ensure the correct operation of the circuit under test right after fabrication, while testing is carried out periodically to ensure that the circuit under test continues to operate correctly on the field. The use of off-line Built-In Self-Test (BIST) techniques for periodic testing imposes the interruption of the normal operation of the circuit under test. On the other hand, the use of input vector monitoring concurrent BIST techniques for periodic testing provides the capability to perform the test, while the circuit under test continues to operate normally.

In this paper, a novel input-vector monitoring concurrent BIST technique for combinational circuits based on a self-testing RAM, termed R-CBIST, is presented. The presented technique compares favorably to the other input vector monitoring concurrent BIST techniques proposed so far with respect to the hardware overhead, and the time required for the concurrent test to be completed (concurrent test latency). R-CBIST can be utilized to test ROM because it results in small hardware overhead, whereas there is no need to stop the ROM normal operation.

Abbreviations and Acronyms 1

AGC Active test set Generator and Comparator
BIST Built-In Self-Test
CTL Concurrent Test Latency
CUT Circuit Under Test
LFSR Linear Feedback Shift Register
MISR Multiple Input Shift Register
ROM Read Only Memory
R-CBIST RAM-based Input Vector Monitoring Concurrent BIST
RV Response Verifier
TPG Test Pattern Generator

With the current trend to dramatically increase the scale of integration, Built-In Self-Test (BIST) techniques provide an attractive solution to test modules deeply embedded in complex integrated Circuits. BIST eliminates the necessity of high-bandwidth test interactions and allows at-speed testing. Other benefits of BIST include reduced product development cycle and cost-effective system maintenance.

BIST utilizes a Test Pattern Generator (TPG) to generate the test patterns which are applied to the inputs of the Circuit Under Test (CUT). In off-line BIST, the normal operation of the CUT is stalled in order to perform the test. Thus, if the CUT is of critical importance for the function of the circuit, the total circuit performance is degraded. To avoid this performance degradation, input vector monitoring concurrent BIST techniques have been proposed which exploit input vectors arriving at the inputs of the CUT during normal operation.

The block diagram of an input vector monitoring concurrent BIST technique is presented in Fig. 1. The CUT is combinational, has \( n \) inputs and \( m \) outputs, and is tested exhaustively; hence, the test set size is \( N = 2^n \). The technique can operate in one out of two modes, normal (when \( TN = 0 \)), and test (\( TN = 1 \)).

During normal mode, the CUT inputs, denoted by \( A = A[n:1] \) are driven from the normal input vector (\( V[n:1] \)). A is also driven to the Active test set Generator and Comparator (AGC), where it is compared to a set of active test vectors called active test set. If it is found that A matches one of the active test vectors, we say that a hit has occurred, or that the input vector \( V \) has performed a hit. When a hit occurs, A is removed from the active test set, and the Response Verifier (RV) captures the CUT response to the input vector. When all input vectors have