Analysis of a Modified Model for Synchronous Multiprocessor Systems

Halatsis, Constantin

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<table>
<thead>
<tr>
<th><strong>Title:</strong></th>
<th>Analysis of a modified model for synchronous multiprocessor systems</th>
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</thead>
<tbody>
<tr>
<td><strong>Year:</strong></td>
<td>1986</td>
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<tr>
<td><strong>Author:</strong></td>
<td>Pombortsis, A., Halatsis, C.</td>
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<tr>
<td><strong>Abstract:</strong></td>
<td>The paper presents an analysis of a modified model for synchronous multiprocessor systems. In this model, besides the shared memory modules, each processor has a private memory. The memory references of each processor are not uniformly distributed among the memory modules, and the rates of request for interconnection varies between 0 and 1 per memory cycle. The interconnection network is considered to be either a crossbar or a shared bus. The performance analysis uses as performance metrics the bandwidth (BW) processor utilization (U) and the memory request completion time (D). Relations among them are derived.</td>
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