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Architectural considerations for a microprogrammable emulating engine using bit-slices

Halatsis, Constantin

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Title: Architectural considerations for a microprogrammable emulating engine using bit-slices

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Author: C. Halatsis, A. Van Dam, J. Joosten, M. Lethern

Abstract: This paper describes architectural considerations which led to the design of a fast programmable processor made from ECL bit-slices. The processor will be used as an on-line data filtering engine for high energy physics experiments. Unlike prior design of such engines, the processor supports both user (horizontal) microcode and emulation of the PDP-11 fixed point instruction set (without memory management and multiple interrupt levels). In addition to an overview of the techniques used to achieve an execution speed of roughly three times that of the PDP-11/70 CPU, strengths and weaknesses of bit-slices and discussed, as are the of a Signetics meta assembler and the ISPS Architecture simulation systems (described in the companion paper "Simulation of a Horizontal Bit-Slice Processor using the ISPS Architecture Facility."